CLOCK GENERATOR WITH PROGRAMMABLE NON-OVERLAPPING-CLOCK-EDGE CAPABILITY

ABSTRACT OF THE DISCLOSURE

A system and method for generating and optimizing clock signals with non-overlapping edges on a chip using a unique programmable on-chip clock generator. Overlapping of the edges of the clocking signals is avoided by adjusting an amount of delay introduced in the on-chip clock generator circuit. The amount of delay is adjusted by programming the on-chip clock generator using either hardware and/or software programming. In hardware programming, the amount of delay adjusted by physically altering the composition of delay elements in the on-chip clock generator. In software programming, the delay is adjusted using software commands to control the operation of delay elements in the on-chip clock generator, or to select the paths that delay the signals.

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